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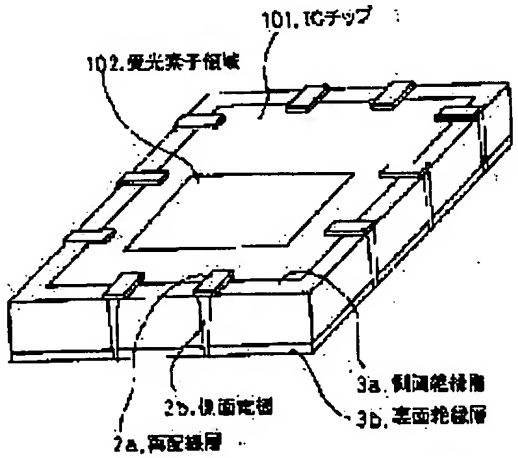
(54) CHIP SIZE PACKAGE AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide the so-called chip size package for inexpensively obtaining a wafer level CSP even to such semiconductor device as a solid-state image pickup element and a photoelectric conversion element by devising the CSP process, and to provide the manufacturing method of the chip size package.
SOLUTION: In the chip size package where a semiconductor integrated circuit and a surface-side electrode are formed on the surface of a chip, a reverse-side insulating layer is formed corresponding to the connection wiring section and at least along the reverse side end, the side insulating layer is formed on the side of the chip so that it is flush with the exposure surface of the connection wiring, and is connected to the reverse side insulating layer, and the surface side electrode is electrically connected to the connection wiring section via the upper end extension section of the connection wiring section being extended to the surface of the chip including the side insulating layer.



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